UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,482	03/12/2004	Akira Takahashi	OKI 414	6303

7590 01/21/2009

RABIN & BERDO, P.C.
Suite 500
1101 14th Street
Washington, DC 20005

EXAMINER	
KRAIG, WILLIAM F	
ART UNIT	PAPER NUMBER
2892	
MAIL DATE	DELIVERY MODE
01/21/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/798,482	TAKAHASHI, AKIRA	
	Examiner	Art Unit	
	William F. Kraig	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,5,11 and 14-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,5,11 and 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2008* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Applicant's amendment of claims 3 and 14-16 and the cancellation of claims 20 and 21 in the response dated 10/31/2008 is acknowledged.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/31/2008 has been entered.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

Therefore, the non-doped polysilicon dummy gate arrangement being etched from a non-doped region of the polysilicon layer wherein an endpoint of the etch is based on the etching of the non-doped polysilicon arrangement of claims 3 and 15 must be shown or the feature(s) canceled from the claim(s). Fig. 3(c) shows no indication that the polysilicon arrangement is etched, which would be an essential feature of the invention given by claims 3 and 15 due to the limitation that the endpoint of the etch is based on the etching of the non-doped polysilicon portion.

No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The amendment filed 3/24/2008 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

The amendment to Fig. 3(c) and the addition of Fig. 4 (both showing an element (labeled "9")) in combination with the modification of the specification to read "the doped polysilicon regions 4 and 5 and the dummy gate electrode region 6 form gate electrodes 7 and 8 and a dummy gate arrangement 9" and "the etched non-doped polysilicon dummy gate pattern" are not supported by the original disclosure. Specifically, there is nothing in the original disclosure which supports there being a structure remaining in the non-doped polysilicon region after the described etching process.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Objections

5. The Examiner's previous objection to claim 21 is withdrawn in light of Applicant's cancellation of claim 21.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. The Examiner's previous rejections of claims 20 and 21, under 35 U.S.C. 112, are withdrawn in light of Applicant's cancellation of claims 20 and 21.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3, 5, 11, 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liau et al. (U.S. Patent # 5783850) in view of Gabriel et al. (U.S. Patent # 6541359) further in view of Lee et al. (U.S. Patent # 5665203) with evidence provided by Lu (U.S. Patent # 4989057).

Regarding claims 3, 5, 15, 18 and 19, Liau et al. discloses a dry etching method for a semiconductor device, comprising the following steps of:

providing a polysilicon layer 26 (Col. 4, Lines 15-20) formed on a silicon substrate 20 (Col. 3, Lines 60-65);

implanting a first region of the polysilicon layer 26 with N type ions (Col. 4, Lines 25-40) and a second region of the polysilicon layer 26 with P type ions (right-most region of Fig. 7), a further region of the polysilicon layer (leftmost region of Figure 7) being left as a non-doped region (Col. 4, Lines 65-67);

forming an N type polysilicon gate electrode 41 from the first region (see middle region of Fig. 7), a P type polysilicon gate electrode 41 from the second region (right-most region of Fig. 7), and a non-doped polysilicon dummy gate arrangement 40 from the non-doped region of the polysilicon layer (left-most region of Fig. 7),

the N type polysilicon gate electrode occupying an area that is smaller than the first area (see Fig. 7), the P type polysilicon gate electrode occupying an area that is smaller than the second area (see Fig. 7).

Liau et al., however, fails to disclose the gate electrodes and the undoped polysilicon body being simultaneously etched during an etching process wherein the etching process includes at least one etching stage in which end point detection is based on the etching of the non-doped polysilicon body or wherein the non-doped polysilicon body occupies an area that is smaller than a total area occupied by the N type polysilicon gate electrode and the P type polysilicon gate electrode.

Gabriel et al. teaches simultaneously gate-etching (Gabriel et al., Col. 7, Lines 6-9) an N type polysilicon gate electrode (Gabriel et al., Fig. 5A (540, 550)), a P type polysilicon gate electrode (Gabriel et al., Fig. 5A (540, 550)) (Gabriel et al., Col. 6, Line 62 – Col. 7, Line 9), and a non-doped polysilicon body (Col. 7, Lines 1-9) during an etching process wherein an end point detection of one of the stages of the etching process is based on the etching of the non-doped polysilicon body (Col. 7, Lines 6-9).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the simultaneous gate etching process of Gabriel et al. into the device of Liau et al. The ordinary artisan would have been motivated to modify Liau et al. in the above manner for the purpose of avoiding microtrenching (Gabriel et al., Col. 2, Lines 35-45) while providing a strong detectable endpoint signal (Gabriel et al., Col. 7, Lines 1-10).

Liau et al. and Gabriel et al., however, fail to disclose wherein the non-doped polysilicon body occupies an area that is larger than a total area occupied by the N type polysilicon gate electrode and the P type polysilicon gate electrode.

It would have been obvious to one of ordinary skill in the art to modify the size of the undoped polysilicon portion of Liau et al. and Gabriel et al. As is taught by Lu, the gate length/channel length of the transistor formed using the undoped portion of polysilicon in the gate is proportional to the breakdown voltage and holding voltage parameters of the device and the gate width/channel width of the transistor formed using the undoped portion of polysilicon in the gate is proportional to the current carrying capability of the device (Lu, Col. 7, Lines 40-55). Therefore, said gate length/channel length and gate width/channel width are considered to be result effective variables where the result is the modification of the breakdown and holding voltage levels of the semiconductor device. The claim to a change in the size of the undoped portion of the polysilicon layer therefore constitutes an optimization of ranges. *In re Huang*, 100 F.3d 135, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996).

Liau et al. and Gabriel et al. (with evidence provided by Lu) disclose the dry etching method (Gabriel et al., Col. 1, Lines 34-38) of claim 15, wherein the etching process includes a stage using a mixed gas of HBr and O_2 (Gabriel et al., Col. 1, Lines 63-65), but fail to disclose the etching process being a two step etching process wherein a second stage of the etch uses a mixed gas of HBr, O_2, and He.

Lee et al. teaches a similar method wherein the gate etching process is a two-step process which uses a first stage atmosphere of HBr, Cl_2 and He and a second stage atmosphere of HBr, 0_2 and He (Lee et al., Col. 2, lines 39-41).

It would have been obvious to one of ordinary skill in the art to incorporate the method of Lee et al. into the method of Liau et al. and Gabriel et al. The ordinary artisan would have been motivated to modify Liau et al. and Gabriel et al. in the above manner for the purpose of forming perfectly vertical gate sidewalls (Lee et al. Col. 2, Lines 23-28).

Regarding claim 11, Liau et al., Gabriel et al. and Lee et al. (with evidence provided by Lu) disclose the dry etching method according to claim 3, wherein the P type polysilicon gate electrode is disposed adjacent the N type polysilicon gate electrode (see Fig. 7 of Liau et al.).

Regarding claim 14, Liau et al., Gabriel et al. and Lee et al. (with evidence provided by Lu) disclose the dry etching method according to claim 3, wherein the nondoped polysilicon dummy gate arrangement is disposed adjacent the N type polysilicon gate electrode (see Fig. 7 of Liau et al.).

Regarding claim 16, Liau et al., Gabriel et al. and Lee et al. (with evidence provided by Lu) disclose the dry etching method according to claim 15, wherein the

nondoped polysilicon dummy gate arrangement is disposed adjacent the N type polysilicon gate electrode (see Fig. 7 of Liau et al.).

Regarding claim 17, Liau et al., Gabriel et al. and Lee et al. (with evidence provided by Lu) disclose the dry etching method according to claim 15, wherein the P type polysilicon gate electrode is disposed adjacent the N type polysilicon gate electrode (see Fig. 7 of Liau et al.).

Response to Arguments

8. Applicant's arguments have been considered but are not found to be persuasive. Applicant argues that it is clear from the specification that dummy gate electrodes would have been formed in the non-doped polysilicon region, even though such a feature is not shown in the original drawings. The Examiner argues that the specification is not clear as to whether or not a non-doped polysilicon structure remains after the etching process. At the top of page 5, the specification recites " wherein a dummy gate made of non-doped polysilicon is disposed for polysilicon gate etching and set so as to take an area larger than the total area of the N type...and P type…gate, followed by patterning of polysilicon gate electrodes." In this passage, the specification seems to be referring to the entire area of non-doped polysilicon (before etching) as the "dummy gate". Further, the bottom of page 6 of the specification refers to Fig. 3c as showing "doped polysilicon regions 4 and 5 in the dummy gate electrode region 6 are etched to form gate electrodes". In Fig. 3c, there are no polysilicon structures showing in the undoped

polysilicon region. Lastly, on page 7 of the specification, the "dummy gate patterns" are defined as being "made of non-doped polysilicon". It is unclear from this whether or not the "patterns" are formed of non-doped polysilicon or the "dummy gates" are formed of non-doped polysilicon. The Examiner thus argues that the specification does not provide sufficient evidence for the inclusion of the new matter.

Applicant further argues that "Gabriel does not each simultaneously etching an N-type gate electrode, a P-type gate electrode and an undoped dummy electrode..." The Examiner argues that Gabriel does teach the etching of N-type polysilicon, P-type polysilicon and undoped polysilicon (see the above rejection) during a gate etching step. Further, Liau et al. discloses the structure containing P, N and Non doped gates.

Applicant further argues that it would not have been obvious to one of ordinary skill in the art to optimize the current carrying capacity of an ESD protection transistor. The Examiner argues that, as is evidenced by Lu, one of ordinary skill in the art would indeed have been motivated as such (Lu, Col. 7, Lines 40-60).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William F. Kraig whose telephone number is (571)272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lex Malsawma/
Primary Examiner, Art Unit 2892

/W. F. K./
01/13/2009
Examiner, Art Unit 2892